Supplementary information for:

Vertical CNT-Si Photodiode Array

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This file includes:

Fabrication Process

Device fabrication begins with the growth of a thermal oxide layer on degenerately doped p-type c-Si substrate, followed by sputtering of 80nm tungsten. In this work nickel is used as the catalyst for the growth of carbon nanotubes (CNTs). By controlling the location and size of the nickel islands it is possible to achieve a regular array of individual, vertically aligned CNTs. Further discussion on CNT's growth is given elsewere[1]. E-beam lithography and lift-off processes are used to pattern catalytic nickel in to islands on the tungsten film. An aluminium film with thickness of 1nm is used between the tungsten and nickel films to prevent interlayer diffusion during the subsequent steps. Following the patterning of nickel islands, direct current (DC) PECVD is used to grow the CNTs, which along with the tungsten film, act as the back electrode of the device. The CNTs were multiwall (MWCNT) and further information about their structure and electrical properties have been reported in earlier works[2,3].

Following the growth of the CNT array, the sample was transferred to a radio-frequency PECVD system for deposition of the p-i-n structure. First a p-type a-SiC:H film with thickness of 25nm is deposited. It should be noted that this thickness corresponds to the thickness of the film deposited on a planar structure. The film thickness measured using SEM on the vertical sidewalls of the CNT suggests that for the deposition conditions used in this work, the vertical film thickness is approximately 3/5 that of the planar film thickness. Therefore the estimated thickness of the p-layer on the sidewalls of the CNT is approximately 15nm. This was followed by deposition of a graded layer consisting of intrinsic a-SiC:H with a planar (vertical) thickness of 5nm (3nm), 250nm (150nm) of intrinsic a-Si:H layer, and 30nm (18nm) of n-type a-Si:H layer.

Following the growth of the p-i-n structure, the sample is transferred to an e-beam evaporator for the deposition of the semi-transparent top electrode, which consisted of Ti and Au films with thicknesses of 1.5nm and 10nm, respectively. The evaporation was done though a shadow mask with dimensions of 3mm x 3mm, which define the device's active area.

The Ti adhesion layer is used to form a smooth interface with the amorphous silicon film, due to its reaction with the SiO_2. Therefore application of the Ti wetting layer prevented formation of small grains associated with thin evaporated Au on silicon and the subsequent high resistance. Indeed, by adopting this approach, a Ti/Au bilayer film with low sheet resistivity of 13 Ω/sq was measured using a 4 point probe on intrinsic a-Si:H coated glass substrate. The Ti/Au film has a peak optical transmission of 47% at 520nm with transmission at blue (400nm) and red (650nm) of approximately 35% as shown in Figure S1.

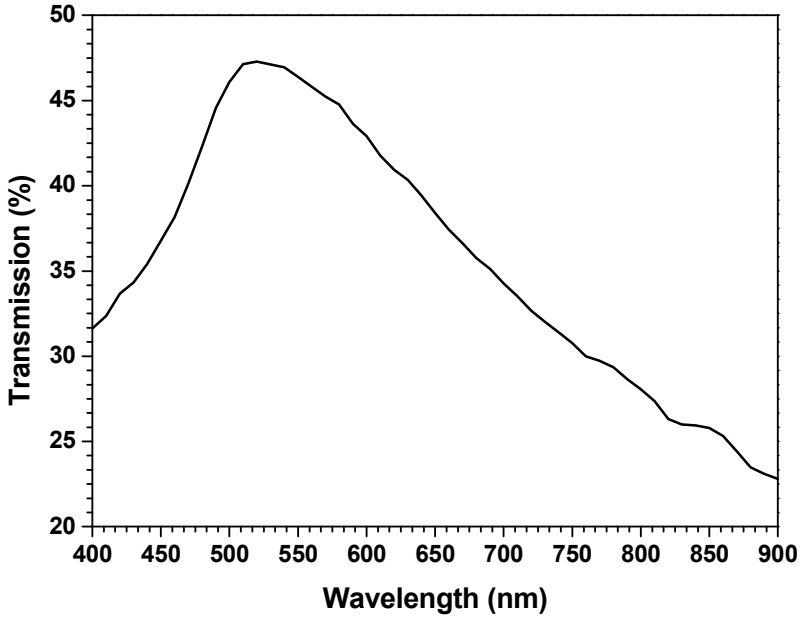

Figure S1. Transmission through Au/Ti.

Experimental Details

All the electrical measurements were performed inside a dark, low noise probe station using the Keithely 4200 semiconductor characterisation system. The illumination source was a halogen microscope light with a radiance of 3mm focused on the sample. The light intensity, measured using a calibrated Newport silicon photodiode was 1.2mW/cm^2 and its spectrum, shown in Figure S2, was measured using a HR200 Ocean Optic spectrometer.

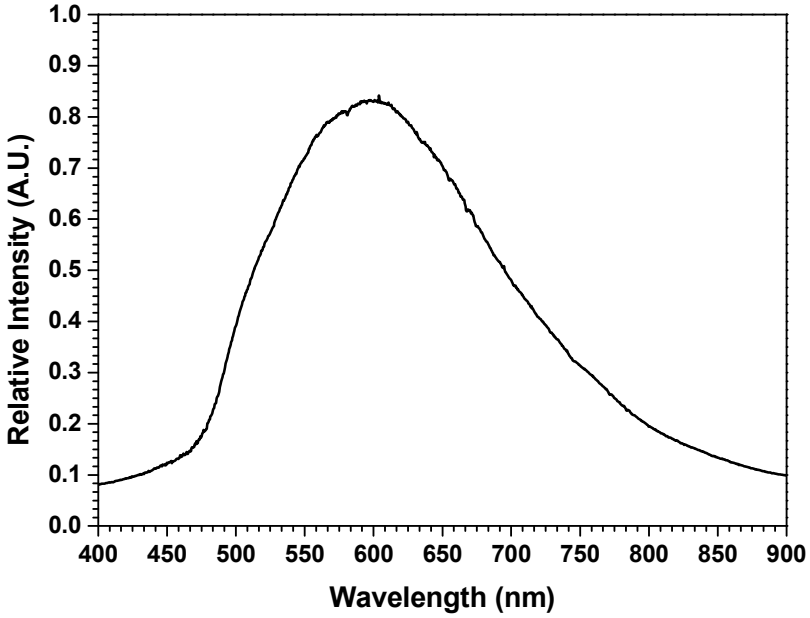

Figure S2. Spectrum of microscope light source.

The conductive tip AFM was performed using a Veeco dimension 3100 using a platinum c-AFM tip with diameter of 20nm. The substrate was grounded relative to the tip by applying silver paste to the metallic AFM table. The series resistance introduced due to the AFM setup was 200Ω. The measurement was performed in two stages. First a topological image of the sample was obtained using contact mode AFM with minimal force to avoid any damage to the sample. This image was used to identify a CNT pillar and using the "point and shoot function" from the operating software, Nanoscope6, its current voltage characteristics where measured. The measurement was performed under illumination of the AFM's optical microscope. However, due to the shadowing effect of the tip, it is not possible to estimate the intensity of the light on the sample.

Junction Capacitance

The capacitance of the photodiode is an important device characteristic in two aspects. Firstly it provides a means of examining the geometric increase in the area of the CNT array photodiode compared with the planar counterpart. Secondly from an application perspective it can be used to estimate the readout time of the photodiode. Figure S3 show the capacitance-voltage characteristics of the device measured in the dark. Given that a large reverse bias current of the CNT array structure leads to errors in the capacitance-voltage measurement (using conversional phase shift type CV meters) we resolved by sputtering a continuous 100nm ITO top electrode (in place of Ti/Au), which supressed this effect. The CNT array and planar photodiodes have capacitances of 44.2 pF/mm^2 and 31.4pF/mm^2, respectively. Therefore CNT array leads to 1.41 times increase in the junction capacitance compared with the planar device.

The capacitance of a cylindrical structure, c, can be calculated using the following equation.

$$C = \frac{2\pi L}{ln\left(\frac{a}{b}\right)} \varepsilon_r \varepsilon_0$$

Here ***L*** is the length of cylinder, ***a*** and ***b*** are the diameters of the outer and inner cylinders respectively. Using this equation, the capacitance of a single CNT pillar photodiode with the height of 0.7um (height of the CNT pillar reduced by the thickness of the p-i-n stack at the bottom of the array), outer cylinder diameter of 190nm (40nm radiance of the CNT pillar plus 150nm thickness of the depletion i-layer on the side wall of the pillar) and inner cylinder diameter of 40nm, can be estimated as:

$$C_{single\ CNT\ pillar} = \frac{2\pi \times 0.7\mu m}{ln\left(\frac{190}{40}\right)} \varepsilon_r \varepsilon_0 = 2.82\mu \times \varepsilon_r \varepsilon_0$$

Based on this the capacitance of the CNT array device can be calculated as:

$$\begin{aligned} C_{CNT\ array\ device} &= C_{planner\ area} + N \times C_{single\ CNT\ pillar} \\ &= \frac{\left((3mm \times 3mm) - \left(300nm^2 \times \pi \times 6.25 \times 10^6\right)\right)}{250nm} \varepsilon_r \varepsilon_0 + \left(6.25 \times 10^6 \times 3.11\mu\right) \varepsilon_r \varepsilon_0 \\ &= 28.9 \varepsilon_r \varepsilon_0 + 17.6 \varepsilon_r \varepsilon_0 = 46.5 \varepsilon_r \varepsilon_0 \end{aligned}$$

Using a simple parallel plate capacitor equation, the capacitance of the planner device can be estimated is

$$C_{planner\ device} = \frac{3mm \times 3mm}{250nm} \varepsilon_r \varepsilon_0 = 36 \varepsilon_r \varepsilon_0$$

Based on this the ratio of the CNT array device capacitance relative to the planar device can be estimated as:

$$\frac{C_{CNT\ array\ device}}{C_{planner\ device}} = \frac{46.5\varepsilon_r\varepsilon_0}{36\varepsilon_r\varepsilon_0} = 1.29$$

This is consistent with 1.41 times increase in the junction capacitance.

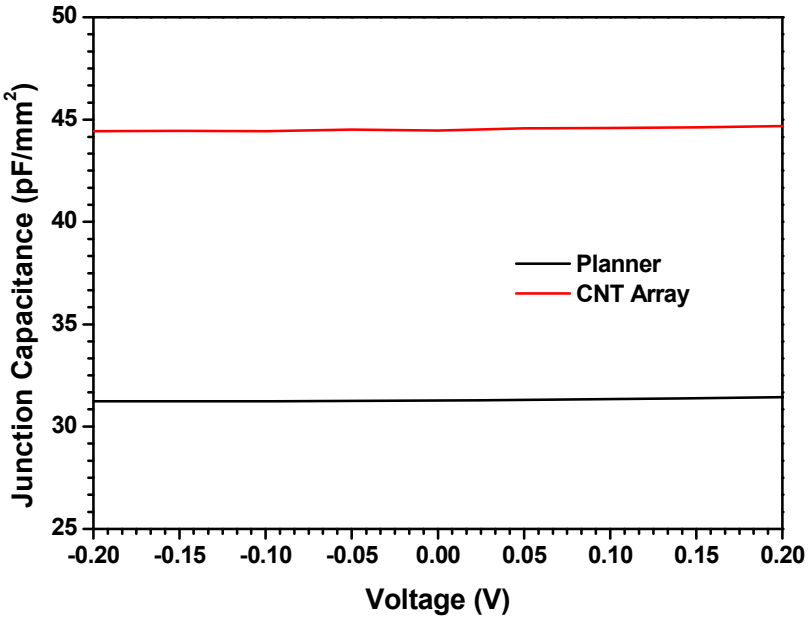

Figure S3 Capacitance-voltage measurement of the planar and CNT array photodiodes.

Electric Field Enhancement

Although earlier works have used CNT array in photovoltaic devices the field enhancement effect have not been observed. The origin of this anomaly is the absence of top electrode on the photodiode pillar's sidewalls, in contrast with the conventional approach of transparent conducting oxide (TCO) sputtering to achieve continuance top electrode. In both approaches field enhancement due to the field-singularity effect associated with convex CNT tip is present. However this enhancement is quenched by TCO encapsulation of photodiode pillars due to the field-divergence effect of the concave TCO shell. This effect is avoided in this work by covering the sidewalls with n-type a-Si:H with thickness less than Debye's screening length (~200nm)[4], and therefore eliminating any reduction in the electric field. This effect is highlighted in Figure 3 of the main manuscript, which compares the electric field distribution in a pillar with metallic size wall compare to a pillar without a metallic sidewall and shows avoiding the use of metallic sidewall leads to an increase in the electric field near n-layer.

Differences in the electric field distribution near the n-layer between the two structures results in differences in the density of electrons near n-layer as shown in Figure S4 a) and b). As shown in Fig S4 a), the use of sidewall leads to the presence of a high density of electrons in the intrinsic layer, unlike the structure without sidewall, where the density of electrons rapidly diminish in the intrinsic layer. Fig S4 b) further highlights this effect by presenting the result of the simulation in a numerical form.

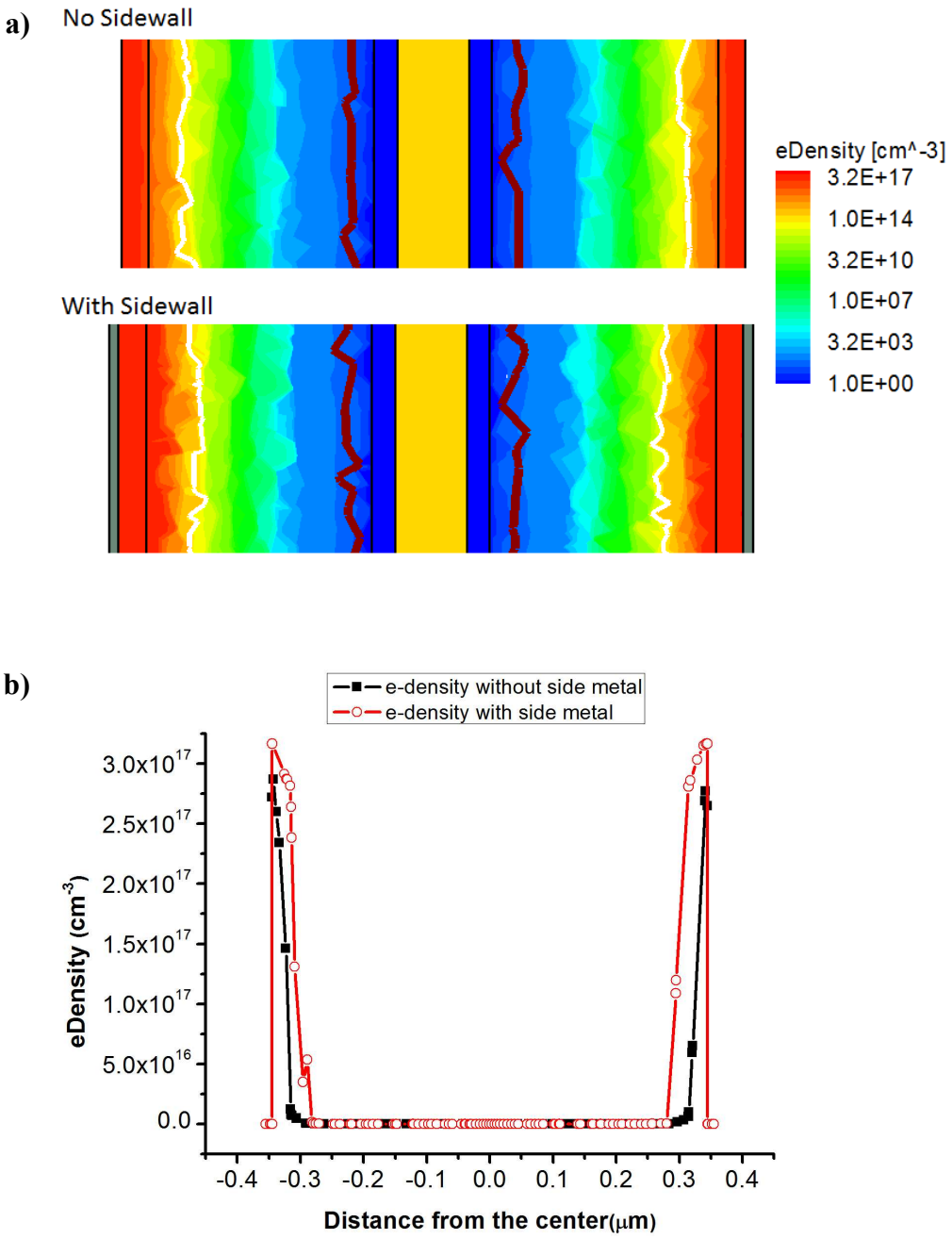

Figure S4 **a)** Cross-sectional diagram of a 3-D electron density profile simulated for two CNT photodiode devices: one with sidewall. Higher density of electrons can be observed near the n-layer for the structure with metallic sidewall. **b)** Numerical representation of the electron density

Optical Enhancement

Figure S5 a) compares the CNT array and planner device's photocurrent under blue (450nm) and red (600nm) illumination. Increase of 35 times and 50 times in the reverse bias photocurrent is observed under blue and red illuminations respectively. This indicates the presence of a limited optical enhancement in at longer wavelengths and is consistent with the devices with similar structures. Figure S5 b) shows the normalized photocurrent spectral response of the of the CNT device biased at zero and -1V. It can be seen that the photocurrent increases at all wavelengths as the bias is changed from zero to

-1V. Furthermore the reduction in the photocurrent at 700nm wavelength (characteristic a-Si:H p-i-n diodes due to the inefficient light absorption at longer wavelengths) cannot be at bias voltage of -1V.

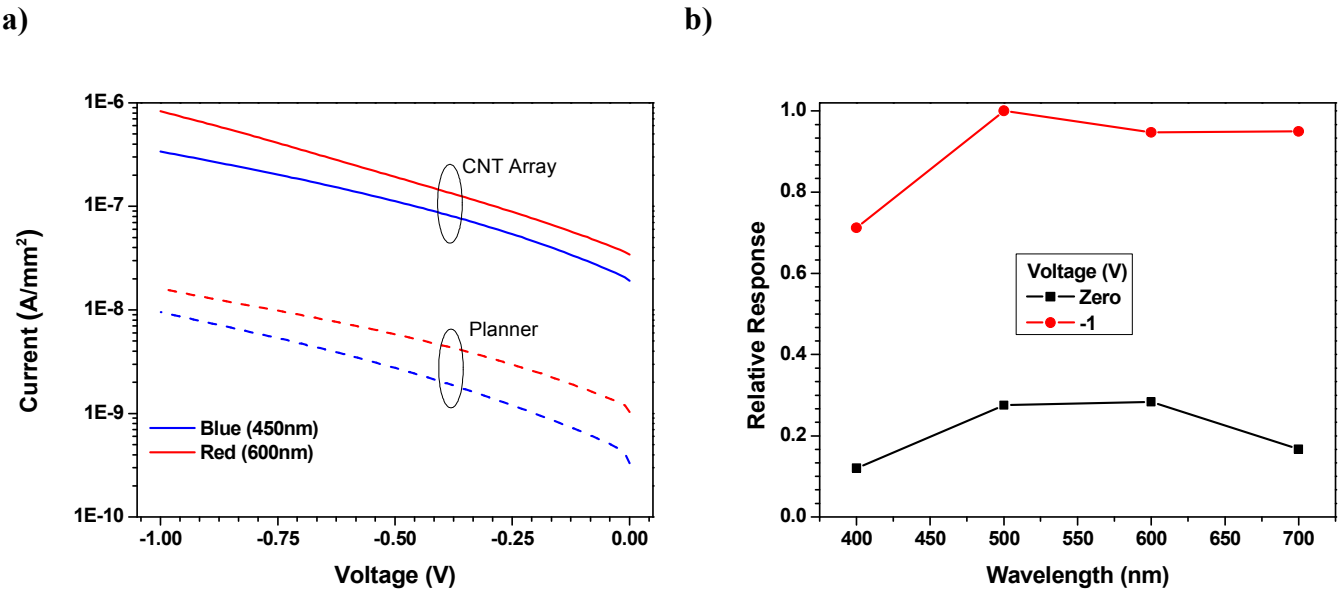

Figure S5 a) Effect of illumination wavelength on the reverse bias photocurrent of the CNT array and planar structure. **b)** Normalised photoresponse of the CNT diode array as a function of bias voltage.

Transient Response

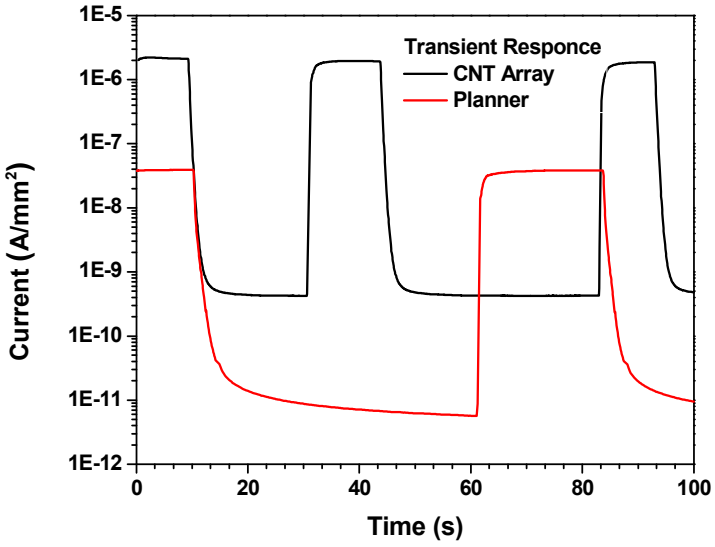

Figure S6 Transient response of planar photodiode and CNT array to pulsed illumination.

System Implication: Flat Panel Imager

Flat panel imagers (FPIs) with high resolution are desirable as they can provide a more detailed image through the use of pixels with smaller area. One of the implications of reduction in pixel size is smaller photodiode area and therefore decreased photocurrent. This reduced photocurrent, especially at lower

light intensities, can reach a stage where it becomes undetectable and comparable to the system noise. The enhancement in CNT photodiode's photocurrent density shown in this work means that device area can be scaled down by a factor of 100 compared with planner structures. Therefore using the CNT-Si photodiode device demonstrated in this work allows a reduction in the current FPI technology with pixel area of $64\mu m^2$ and 100% fill factor to one nano-pillar per pixel.

As well as increase in the FPI resolution, the use of smaller pixels leads to a reduction in the photodiode's parasitic capacitance, which has important implications on the operation of FPI. Figure S4 shows an schematic of a passive pixel sensor architecture. The pixel consists of of a photodiode, a storage capacitor (C_{ST}) and a thin film transistor (TFT_{READ}). At the FPI periphery column charge amplifiers (consisting of an operational amplifier and C_{INT} capacitor) convert the photodiodes' generated charge to output voltage. In the detection mode TFT_{READ} is switched off and the charge generated by the photodiode is accumulated in the pixel. The total pixel capacitance (C_{PIXEL}) is the sum of C_{ST}, parasitic capacitances of the photodiode and the TFT_{READ}. In the integration mode, the TFT_{READ} is switched allowing the stored charge to transfer to the column charge amplifier. The RC time constant associated with the charge transfer process is a function of C_{PIXEL} and TFT_{READ}'s resistance and therefore any reduction in C_{PIXEL} leads to a lower time constant and faster charge transport. For this reason in many FPI design's C_{ST} is not used and therefore $C_{PIXEL} \approx C_{TFT} + C_{PHOTODIODE}$. Based on the junction capacitance of $44pF/mm^2$ and device size of $0.64\mu m^2$, photodiode capacitance of 28aF can be extracted far less that the TFT's parasitic capacitance of 32fF. Assuming TFT's resistance of 23.6MΩ, the pixel read time constant reduces to 755ns. The order of magnitude faster photodiode transient response as well as faster read time enables high-speed operation of the detector without any significant image lag effect.

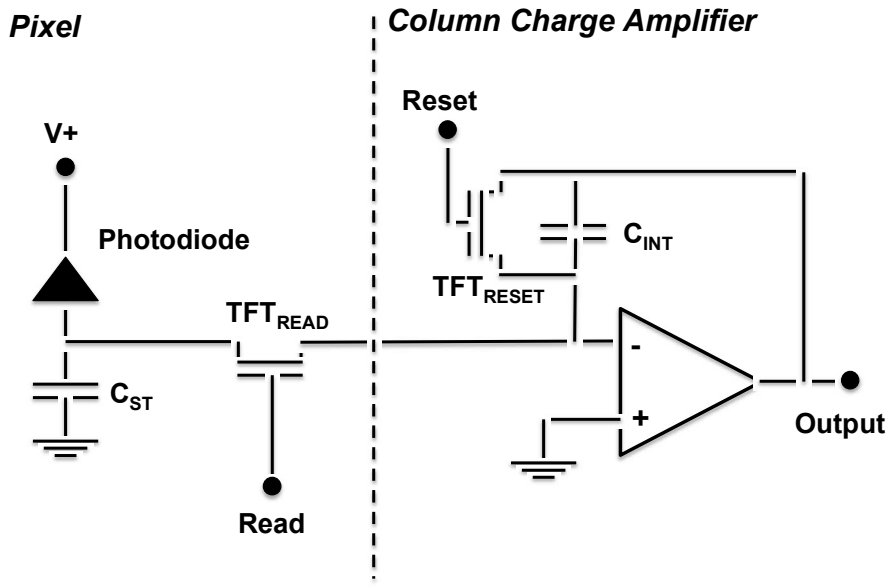

Figure S7 Circuit example used in readout.

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